Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Cancelled)

Claim 2 (Cancelled)

Claim 3 (Cancelled)

Claim 4 (Cancelled)

Claim 5 (Cancelled)

Claim 6 (Cancelled)

Claim 7 (Cancelled)

Claim 8 (Cancelled)

Claim 9 (Cancelled)

Claim 10 (Currently amended) An anti-fuse memory array comprising:

a plurality of anti-fuse transistors arranged in rows and columns, each anti-fuse transistor including

a polysilicon gate over a channel region in a substrate, the channel having a preset length;

a diffusion region proximate to a first end of the channel region;

a variable thickness gate oxide between the polysilicon gate and the substrate, the variable thickness gate oxide having a thick gate oxide portion extending from the first end of the channel region to a predetermined distance of the preset length, and a thin gate oxide portion extending from the predetermined distance to a second end of the channel region,

an oxide breakdown zone proximate to the second end of the channel region fusible to form a conductive link between the polysilicon gate and the channel region;

bitlines coupled to the diffusion regions of a column of anti-fuse transistors;

a sense amplifier coupled to a pair of the bitlines through isolation devices;

and,

wordlines coupled to the polysilicon gates of a row of anti-fuse transistors.

Claim 11 (Cancelled)

Claim 12 (Currently amended) The anti-fuse memory array of claim 10 [[11]], further including wordline decoding circuitry for selectively accessing one anti-fuse transistor coupled to one of the pair of bitlines for a single-ended sensing operation, and for selectively accessing another anti-fuse transistor coupled to the other of the pair of bitlines for a different address.

Claim 13 (Currently amended) The anti-fuse memory array of claim 10 [[11]], further including wordline decoding circuitry for selectively accessing one anti-fuse transistor coupled to one of the pair of bitlines and one anti-fuse transistor coupled to the other of the pair of bitlines for a dual-ended sensing operation.

Claim 14 (Previously presented) The anti-fuse memory array of claim 10, further including column select pass gates coupled to the bitlines, at least one of the column select pass gates having a gate oxide corresponding to the thick gate oxide portion.

Claim 15 (Cancelled)
Claim 16 (Cancelled)
Claim 17 (Cancelled)
Claim 18 (Cancelled)
Claim 19 (Cancelled)
Claim 20 (Cancelled)
Claim 21 (Cancelled)
Claim 22 (Cancelled)
Claim 23 (Cancelled)
Claim 24 (Cancelled)
Claim 25 (Cancelled)
Claim 26 (Cancelled)
Claim 27 (Cancelled)
Claim 28 (Cancelled)
Claim 29 (Cancelled)
Claim 30 (Cancelled)
Claim 31 (Cancelled)